**CS-322 Lab 10**

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# Task 1

**Study the given piplelined mips implementation of the processor and test using the following test program (create a new mem.dat)**

**Code:**

***add*** *$s0, $0, $0*

***add*** *$s1, $0, $0*

***addi****$t0, $0, 10*

*loop:*

***slt*** *$t1, $s0, $t0*

***beq*** *$t1, $0, done*

***add*** *$s1, $s1, $s0*

***addi*** *$s0, $s0, 1*

***j****loop*

*done:*

**Machine Code:**

00008020

00008820

2008000A

0208482A

11200003

02308820

22100001

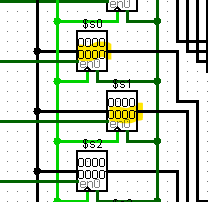
08000003

**Algorithm:**

Given algorithm adds the first n whole numbers. Going from s0 = 0 to s0 = 9 and adds s0 to s1.

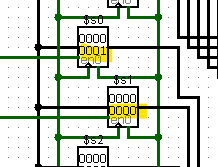
**Execution**

Before execution



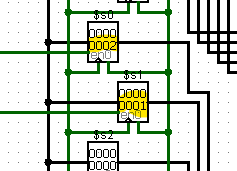
Nothing initially stored in the registers

1st iteration



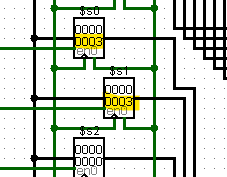
S0 updated to 1 and s1 = s1 + 0

2nd iteration



S0 updated to 2 and s1 = s1 + 1

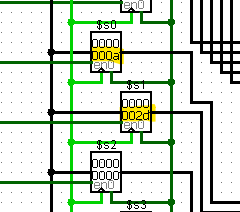
3rd iteration



S0 updated to 3 and s1 = s1 + 2

And so on

After completion of complete execution



S0 = 10 and s1 = sum of first 9 numbers (0x2d = 45).

**Note**: There was a mistake in the logic circuit of the Control Decoder, which gave the wrong control signals for Addi. I have built another circuit to incorporate the change and ran the program using it.

# Task-2

Number of cycles in Single cycle architecture = 55

Number of cycles in Multi cycle architecture = 199

Number of cycles in Pipelined architecture = 128

CPI of Single cycle architecture = = 1

CPI of Multi cycle architecture = = 3.62

CPI of Pipelined architecture = = 2.33

|  |  |  |
| --- | --- | --- |
| Labels | Instruction | Execution Count |
|  | Add $s0, $0, $0 | 1 |
|  | Add $s1, $0, $0 | 1 |
|  | Addi $t0, $0, 10 | 1 |
| Loop: |  |  |
|  | Slt $t1, $s0, $t0 | 11 |
|  | Beq $t1, $0, done | 11 |
|  | Add $s1, $s1, $s0 | 10 |
|  | Addi $s0, $s0, 1 | 10 |
|  | J loop | 10 |
| Done: |  |  |
| Total Number of Instructions executed |  | 55 |